10. (currently amended) The eDRAM device of claim 9, ~~further comprising a~~ wherein said plurality of deep trench isolations surrounding said memory storage region.

11. (cancelled)

12. (original) The eDRAM device of claim 11, wherein said memory storage region includes a plurality of deep trench storage capacitors.

13. (original) The eDRAM device of claim 12, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.

14. (withdrawn) A method for blocking the propagation of defects generated in a semiconductor device, the method comprising:

forming a deep trench isolation formed between a memory storage region of the semiconductor device and a logic circuit region of the semiconductor device; said deep trench isolation being filled with an insulative material;

wherein said deep trench isolation prevents the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region.

15. (withdrawn) The method of claim 14, wherein said deep trench isolation is formed beneath a shallow trench isolation, said shallow trench isolation for electrically isolating devices contained in said memory storage region from devices contained in said logic circuit region.